**PATENT** Atty Docket No.: 10004741-1

App. Ser. No.: 09/915,531

**IN THE DRAWINGS:** 

The attached sheets of drawings include changes to Figs. 1, 2A and 2B. These sheets,

which include Figs. 1, 2A and 2B, replace the original sheets including Figs. 1, 2A and 2B. In

each of Figures 1, 2A and 2B, the legend "Prior Art" has been added.

**IN THE SPECIFICATION:** 

Please replace the paragraph starting at page 2, line 11 with the following amended

paragraph:

[Figure 2 illustrates] Figures 2A and 2B illustrate setup and hold times for the case

where the sink is a latch. Figure 2A shows a dynamic latch 200 accepting an input D and a

clock signal CLK. The dynamic latch 200 produces an output Q, which follows the input D,

after a small delay, when the clock signal CLK is high and remains in the same state when

the clock signal CLK is low. Figure 2B shows waveforms of the clock signal CLK, the input

D and the output Q. As shown in Figure 2B, the input D pulses high briefly. In order for the

output Q to follow the input D, the input pulse must be high for a setup time T<sub>S</sub> before the

clock signal CLK falls low and stay high for a hold time T<sub>H</sub> after the clock signal CLK falls

low. The setup time T<sub>S</sub> or the hold time T<sub>H</sub> may be violated if the clock signal CLK drifts, as

can happen when there is excessive clock skew.

2